amplitude signal, the phase signal, and one or more signs of the two parallel sigma delta modulators outputs.

16. The apparatus of claim 15, wherein the apparatus is further configured to at least choose the feedback gain proportional to a rectangular domain change equivalent of least significant bit changes of the amplitude signal and the phase signal.

17. The apparatus of claim 15, wherein the apparatus is further configured to at least choose from one or more gain levels, one of the gain levels providing a high gain in the two parallel sigma delta modulators.

18. The apparatus of claim 14, wherein the two sigma delta modulators have different non-even quantizer levels, and wherein the non-even quantizer levels are adaptively chosen according to at least the amplitude signal, the phase signal, and the one or more signs of the two parallel sigma delta modulators outputs.

19. The apparatus of claim 18, wherein the apparatus is further configured to at least choose the non-even quantizer levels, such that the non-even quantizer levels are propor-

tional to rectangular domain change equivalents of one or more least significant bits changes of the amplitude signal and the phase signal, wherein the first and second noise is due in part to at least one of a regular or an irregular step size of quantized polar domain signals.

20. A non-transitory computer-readable storage medium including computer program code, which when executed by at least one processor circuitry causes operations comprising:

receiving a first error signal representative of a first noise including a first quantization noise carried by a quadrature signal;

receiving a second error signal representative of a second noise including a second quantization noise carried by an in-phase signal; and

determining one or more bits in a polar domain, wherein the one or more bits cancel a portion of the first noise and the second noise represented by the first error signal and the second error signal.

21. (canceled)

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